International Journal of Electronics and Communication Engineering (IJECE)
ISSN(P): 2278-9901; ISSN(E): 2278-991X
Vol. 2, Issue 5, Nov 2013, 107-112

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

VLSI BASED DESIGN OF BULK DRIVEN OPERATION AMPLIFIER

PRAMOD KUMAR JAIN, D. S. AJNAR & RANJEET KUMAR SAHU

Department of Electronics & Instrumentation Engineering, Shri G. S. Institute of Technology and Science, Indore, Malwa, Madhya Pradesh, India

ABSTRACT

Low-voltage, low-power consumption is a desirable feature for any portable electronic device for longer battery life, prevent chip overheating, shrinking the battery size and its weight as well. In present paper, Operational Amplifier is designed using the Bulk-Driven technique, the input signal is applied to the body terminal. This operational amplifier has been operated at 0.8 V, and consume power 146.789 µW which is less than earlier design. So it can be considered as ultra Low Voltage, Low Power design.

In the aim to enhance the performance of the proposed Bulk-driven circuit, the self-cascode structure is employed. The self-cascode structure increases the performance of the circuit furthermore. it is suitable for Low Voltage circuit designs. Open loop gain is obtained as 87.39 dB with phase margin of 77.25 dB. All simulations of the design are carried out in the Cadence tool with 0.18 µm Technology.

KEYWORDS: Low-Voltage, VLSI, Operational Amplifier

INTRODUCTION

The gate-driven CMOS operational amplifiers are not sufficient for operation under very low supply voltages due to limited threshold voltage. Many low voltage techniques with addition to gate-driven amplifiers have been proposed [1-3]. The bulk-driven differential operational amplifier topology those using positive feedbacks for voltage gain boosting of an amplifier. transistor is a good solution to overcome the threshold voltage Limitation. It can work under negative, zero, or even slightly positive biasing conditions [4]. The square law equation for the PMOS transistor in saturation can be applied in Eq. (1) to describe the relationship between the output drain current (I_D) and the bulk-to-source voltage (V_{BS}) without any channel length modulation

$$I_D = \frac{1}{2}\beta\left(V_{SG} - V_{THO} - \gamma_P\left(\sqrt{2\emptyset_F + V_{BS}} - \sqrt{2\emptyset_F}\right)\right)^2 \quad (1)$$

Where V_{THP0} is the threshold voltage of PMOS at zero substrate voltage, φ_F is the bulk Fermi potential, γ_P is a constant describing the substrate bias effect, V_{SG} is the source-to-gate voltage. The bulk transconductance g_{mb}

$$g_{mb} = \frac{dI_D}{dV_{BS}} = \left|-\beta\left(V_{SG} - V_{THO} - \gamma_P\left(\sqrt{2\emptyset_F + V_{BS}} - \sqrt{2\emptyset_F}\right)\right)\frac{\gamma_P}{2\sqrt{2\emptyset_F + V_{BS}}}\right| \quad (2)$$

where g_{mb} can be further related to g_m in Eq.

$$g_{mb} = g_m \frac{\gamma_P}{2\sqrt{2\emptyset_F + V_{BS}}} = g_m.\eta \quad (3)$$

the ratio of g_{mb} to g_m only ranges from 0.2 to 0.4 depending on the bulk-to-source voltage and the specific process parameters [8-9].

DESIGN OF OPERATIONAL AMPLIFIER

The proposed bulk-driven differential operational amplifier is shown in Figure 1. The bulk driven differential input pair M_{1A-B} with the conjunction of the common-gate transistors M_{2A-B} constructs the input stage of the amplifier. The first voltage gain stage is realized by the folded cascode transistors M_{3A-B} and M_{6A-B}. The second voltage gain stage is constructed by the common-source transistors M_{7A-B} and M_{8A-B}. The RC networks are used for the frequency compensation of the differential amplifier. Transistors M_{5A-B}, and $M_{4,4A-B}$ form the current mirrors that bias the input stage. The constant voltages vbp1, vbn1, vbp2 and vbn2 are produced by the biasing circuit, shown in Figure 2. The voltages vbp2 and vbn1 have the appropriate values in order to force the drain-to-source voltage of transistors M_{5A-B} and M_{4A-B} to be about 150 mV, operating at the edge of the strong inversion [3]. The control voltage V_{CMFB} that fed the gate terminals of M_{6A-B} is produced by the output of the common- mode amplifier (Figure 3).

Thus, input bulk-driven transistors M_{1A-B} are involved into the positive feedback loop, as well. Based on small signal equivalent circuit of the amplifier's input stage and neglecting the channel conductance of M_{1A-B} and M_{2A-B}, the effective transconductance will be given by

$$g_{m,eff} = g_{mb1}\frac{g_{mb2}+g_{m2}}{g_{mb2}+g_{m2}-g_{m1}} \quad (4)$$

Where g_{mb1}, g_{m1} are the bulk and gate-transconductance of M_{1A-B}. g_{mb2} and g_{m2} are the bulk and gate transconductance of M_{2A-B}. According to Eq.4,

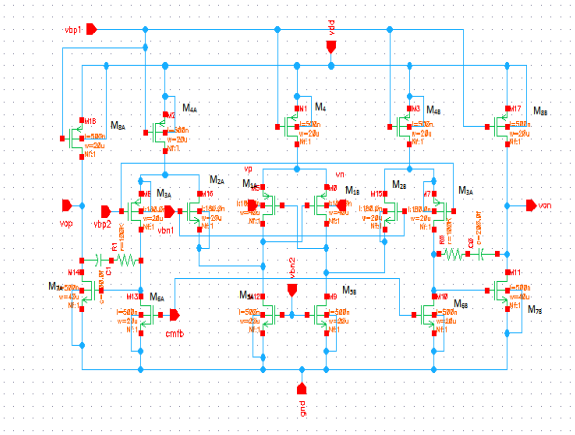

Figure 1: The Schematic Design of the Proposed Bulk-Driven Operational Amplifier

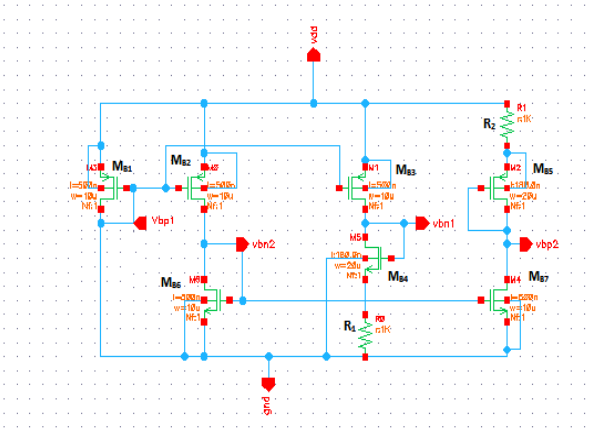

Figure 2: Schematic Design Bulk-Driven Circuit

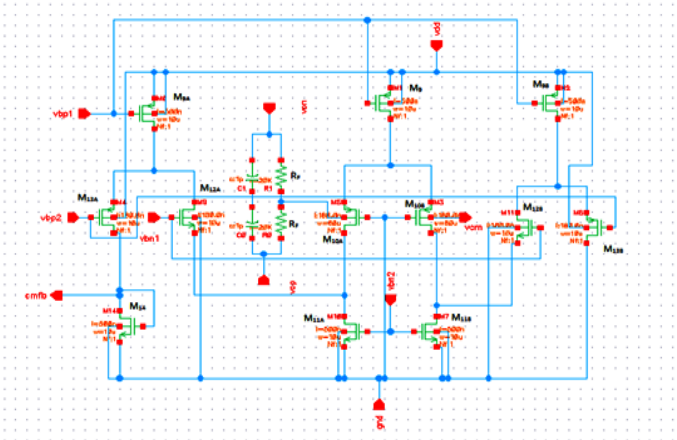

Figure 3: Schematic Design of Common Mode Feedback Amplifier Circuit

SIMULATION RESULTS

In this chapter the schematic of the circuit has been tested for various parameter of operational amplifier. The amplifier is powered by supply voltage 0.8 V. The fully differential bulk driven CMOS op-amp has been designed and simulated on cadence tool 0.18um technology

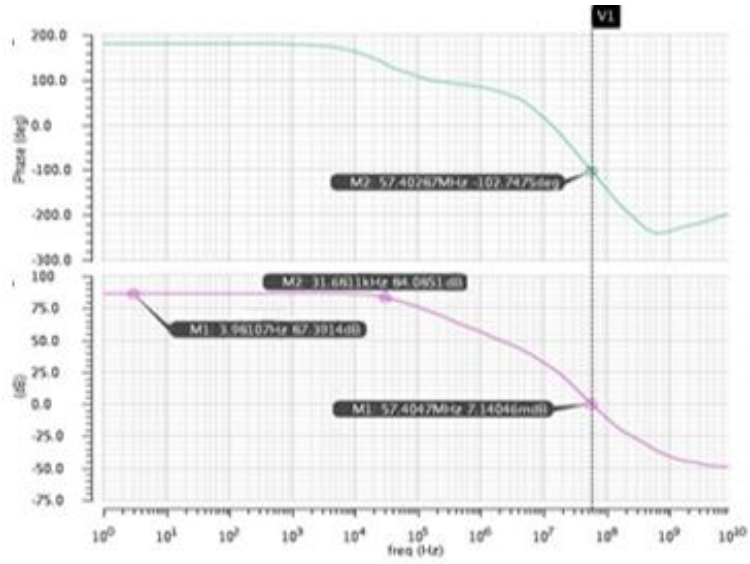

Figure 4: Frequency Response Plot with Load C_L=5pf

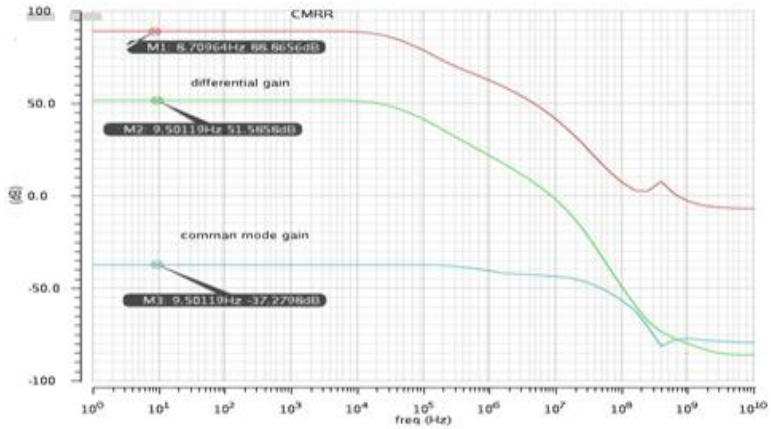

Figure 5: CMRR at 27^{o}C with C_L = 5pf

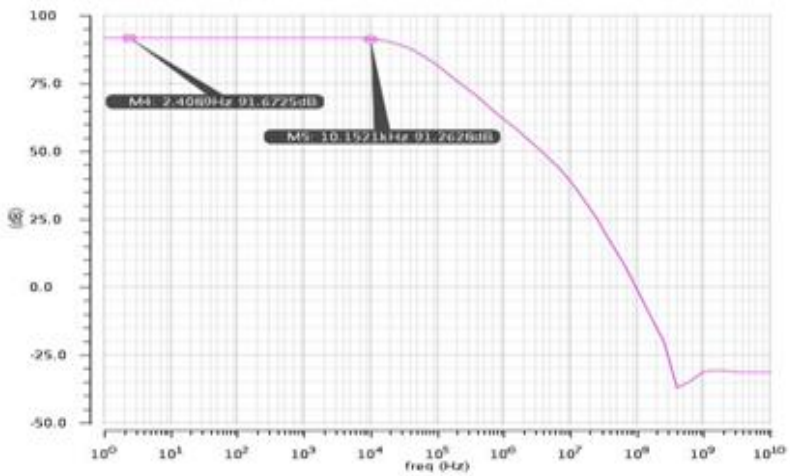

Figure 6: PSRR at 27^{o}C

Table 1: Simulation Results of Bulk Driven Operational Amplifier

S. No.	Parameters	Simulation Results
1	DC gain (dB)	87.39dB
2	Unity gain bandwidth (MHz)	57.404M Hz
3	Phase margin	77.25^{o}
4	F_{3dB} frequency range	31.681 KHz.
5	CMRR	88.8656dB
6	PSRR	91.67dB
7	Power dissipation (µW)	146.789
8	Area(µm*µm)	70716.488

CONCLUSIONS

In this paper present a bulk driven operational amplifier topology for low power and low voltage. This op amp can be used in High CMRR and PSRR applications such as bio-potential amplifier and small battery operated devices. It is the schematic of CMOS operational amplifier has Open Loop Gain 87.39dB and unity gain frequency obtained is 57.404MHz. The phase margin obtained is 77.25^{o}. PSRR recognized that the change in output with supply voltage is 91.67dB. The common mode rejection ratio was found to be 88.8656dB and bandwidth 31.681 KHz, Power Dissipation is 146.789 µW. Then, finally designed Layout of Bulk Driven Differential Amplifier.

REFERENCES

1. B. J. Blalock, , P. E. Allen, G.A. Rincon-Mora, Designing 1-V op amps using standard digital.
2. Carrillo, J. M., Torelli, G., Pirez-Aloe, R., & Duque-Carrillo, J. F. (2007). 1-V rail-to-rail CMOS opamp with improved bulk-driven input stage. IEEE International Journal of Solid-State Circuits, 42(3), 508–517.
3. Haga, Y., Morling, R. C. S., & Kale, I. (2006). A new bulk-driven input stage design for sub 1-Volt CMOS Op-Amps. In Proceedings of IEEE international symposium on circuits and systems (ISCAS) (pp. 1547–1550).
4. G. Raikos, S. Vlassis, "0.8 V bulk-driven operational amplifier," Analog Integrated Circuits and Signal Processing, vol.63, no.3, pp. 425-432, 2009.
5. Ferreira, H. C. L., Primenta, T. C., & Moreno, R. L. (2007). An ultra-low-voltage ultra-low-power CMOS MIller OTA with railto- rail input/output swing. IEEE Transactions on Circuits and Systems II, 54(10), 843–847.
6. Raikos, G. S. Vlassis, "Low-voltage bulk-driven input stage with improved transconductance," International Journal of Circuit Theory and Applications, vol. 39, no.3, pp. 327-339, 2011.
7. Haga, Y., & Kale, I. (2009). Bulk-driven flipped voltage follower. In Proceedings of IEEE international symposium on circuits and systems (ISCAS) (pp. 2717–2720).

AUTHOR'S DETAILS

Pramod Kumar Jain received the Bachelor of Engineering (B.E.) degree in Electronics and communication Engineering in 1987 and Master of Engineering (M.E.) Degree in Electrical Eng. Specializing in Digital Techniques & Instrumentation Engineering in 1993, both from S.G.S.I.T.S affiliated to Devi Ahilya Vishwavidyalaya (formally known as University of indore) Indore, India. He has been teaching and in R and D profession since 1988. Presently he is working as Associate professor in Department of Electronics & Instrumentation Engg., S.G.S.I.T.S. Indore India. His research interest include device modeling and ultra large scale IC technology..

D. S. Ajnar Received B.E. degree in Electronics and Communication Engineering from D.A.V.V. University, India in 1993 and M.E. Degree in Digital Techniques & Instrumentation Engineering from Rajiv Gandhi Technical University Bhopal, India in 2000. He has been teaching and in research profession since 1995. He is now working as Reader in Department of, Electronics & Instrumentation Engineering S.G.S.I.T.S, Indore, India. His interest of research is in Designing of Analog filter and current conveyors.

Ranjeet Kumar Sahu received the B.E. degree in Electronics and Communication Engineering from Barkatullah University, Bhopal in 2008. Currently Pursuing Master of Technology in Microelectronics and VLSI Design from S.G.S.I.T.S., Indore. His Research Interest includes Analog Filter Design and low power Audio Amplifier.